<u>Proposal for announcing seat under the Institute Internship Program</u>

(separate form to be filled for seat under Institute funding and project funding)

1. Name of faculty member proposing: **Menka**
2. Department/Centre- ECE
3. Topic on which work is proposed: Digital/Analog circuit design

4. Preferred period of internship (after May 20th): Between **21st May 2024 to 5th July 2024**

5. Qualification of student (branch/semester of study): UG – ECE/CSE/EE- 5th/7th semster

6. Brief description of work (300-500 words): Designing digital logic circuits using Verilog. Writing Testbench for these and synthesizing to get final details of the design.

    Designing Analog circuits –like- amplifier, LDO, ADC etc. And getting layout details.

7. Expected learning of student (upto 100 words): Complete flow of Analog/Digital design. Various steps involved to improve the design and make it as much close to specifications as possible.

8. Nature of work: (Experimental/simulation/mathematical modelling/data collection-analysis etc.): upto 50 words- **Simulation and Modeling**

9. If the seat is under project sponsored category: Yes/**No**
    a) If yes, number of seats announced:
    b) Name and ID no. of project from which stipend is chargeable

Menka

Signature of faculty member

Name of department/Centre

Electronics and Communication Engineering

Note:

a) Proposing faculty member needs to be available at the Institute during the period internship is offered
b) No extra space or funding than the stipend will be provided by the institute for this purpose