No.:IIITK/2022-23/R&D/616   **Date: 06.03.2023**

Advertisement for the Post of Project Staff (JRF) (Purely on Contract)

Applications are invited from Indian nationals for the post of **Junior Research Fellow (JRF)** on contract in a research project entitled "**Simulation Analysis and Implementation of Soft Decision Forward Error Correction Codes for High-Speed Free-Space/Satellite Optical Communication**" sponsored by the Indian Space Research Organization (ISRO). The post is purely on a contract basis with an initial appointment for a period of one year (likely to be extended yearly for a period of a maximum of two more years or project duration whichever is earlier subject to the satisfactory performance of an individual).

All the applicants need to fill out the application form given at https://forms.gle/dz4p3TKVpFnMJudT7. A soft copy of the duly completed application (scanned) in the prescribed format (Annexure-1), detailed CV, and self-attested photocopy of all the supporting documents should be uploaded on the given link latest by *April 05, 2023* (one month from the date of publishment). Shortlisted candidates will have to appear for the interview at IIIT Kota (MNIT Campus Jaipur) in offline mode.

Designation	Consolidate Payment	No. of position	Educational Qualifications
Junior Research Fellow **(JRF)**	Rs 31,000/- + HRA as per Institute norms	01	**Essential: -** First Division in B.E. / B.Tech. (Electronics and Communication Engineering or any relevant field) or First Division in M.E./ M.Tech. (Electronics and Communication Engineering or any relevant field). **Desirable: -** Prior knowledge/ experience in some areas of Matlab, Xilinx FPGA, Vivado, and basic understanding of Error Correcting Codes and Optical Communication.

Important Instructions for Candidates:

1. The applicant will be responsible for the authenticity of information, other documents and photographs submitted.
2. Mere, possessing the prescribed qualification does not ensure that the candidate would be called for Interview. The Candidates will be shortlisted on the basis of merit and need of the project. IIIT Kota reserves the right to fix suitable criteria for short-listing of eligible candidates.
3. Only shortlisted candidates will be informed about the interview by e-mail/Mobile and no separate interview letter will be issued for the same. So, the candidate must provide valid E-mail IDs in their applications.
4. Candidates should appear for the interview at their own cost along with their original certificates on the announced date and time.
5. The selected candidate may be allowed to register for the Ph.D. program in the Dept of ECE, IIIT Kota as per institute norms.

Dr. Amit Kumar Garg (PI)
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MNIT Jaipur, Rajasthan

Annexure-1

Application Performa

Project Staff for
ISRO- RACS funded Project, on "Simulation Analysis and Implementation of Soft Decision Forward Error Correction Codes for High-Speed Free-Space/Satellite Optical Communication"

For Office Use	
Serial No: _____	**Self-Attested Photograph**
Eligible: Yes/No___Called for Interview: _____	
Checked the Certificates: _____	

1. Name: ………………………………………………………………………………………

2. Father's Name: ………………………………………………………………………………..

3. Date of Birth: ………………………………………………………………………………

4. Contact information:

    (i)Telephone with STD Code: …………………….. (ii) Mobile No: ………………………….

    (iii) Address for communication …………………………….………………………………....
    ……………………………………………………………………………………….……

    (iv) Email ID: ……………………………………………………………………….…….

5. Educational Qualifications

Class Name	Name of Board/University	Name of School/College/ Institute	Marks/ CGPA	Year of passing
Xth				
XIIth				
B.E./B.Tech				
M.Tech.				
Any other (Please specify__)				

6. (a) Whether GATE/ JRF/NET qualified_____ (Please specify along with the year of award)

7. Total Experience (in years)…………………………

SN	Organization	Designation	Duration	Responsibilities
1				
2				
3				
4				

8. Publications: (Attach separate sheet indicating SCI, Scopus indexed for details)

    National (Nos)………………………   International (Nos)……………..…....…….…

9. Workshop/Training programs attended………………………………………………..…..

10. Other qualifications/Certified course/relevant information/achievements if any

SN	Details
1	
2	
3	
4	
5	

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11. State how you are previously engaged in Matlab, Xilinx FPGA, Vivado, Error Correcting Codes and Optical Communication (a separate sheet may be attached if required).

I have provided correct information as above and I understand that, if found incorrect, I may be disallowed to appear in Interview/Test.

Place:

Date: **Signature of Applicant with Name**

Note:

- Please attach self-attested photocopy of supporting documents for column 5 to 10 along with application form.
- Original Certificates for verification with one photocopy to be brought at time of interview only.