Malaviya National Institute of Technology

Department of Electronics and Communications

Jawahar Lal Nehru Marg, Jaipur-302017

PhD Domain:VLSI & Embedded Systems

Section 1: Electronic Devices

Basic Semiconductor Physics and Devices: p-n junction and metal-semiconductor junction: Zener diode, Diode circuits, BJT, MOSFETs and Advanced VLSI technology

Section 2: Analog Circuits

Diode circuits: clipping, clamping and rectifiers.

BJT and MOSFET amplifiers: biasing, ac coupling, small signal analysis, frequency response. Current mirrors and differential amplifiers.

Op-amp circuits: Amplifiers, summers, differentiators, integrators, active filters, Schmitt triggers and oscillators.

Section 3: Digital Circuits

Number representations: Binary/Octal/Hex Number representation,Fixed and Floating-point arithmetic, Boolean algebra, Optimization of Boolean function, logic gates

Combinationalcircuits: adders/subtractors, multiplexers/demultiplexers, encoders/decoders. comparators.

Sequential circuits: basics of latches and flip-flops, shift-registers, counters, finite state machines, propagation delay, setup and hold time, critical path delay.

Data converters: sample and hold circuits, ADCs and DACs.

Semiconductor memories: ROM, SRAM, DRAM.

Computer organization: Machine instructions and addressing modes, ALU, data-path and control unit, instruction pipelining.

Digital arithmetic: Unconventional number system, Residue number system, logarithmic number system, Chinese Number Theorem

Section 4: Embedded Systems

Embedded computing- Microprocessors, embedded design process, system description formalisms. Instruction sets- CISC and RISC; CPU fundamentals- programming I/Os, co-processors, supervisor mode, exceptions, memory management units and address translation, pipelining, super scalar execution, caching, CPU power consumption. Embedded computing platform- CPU bus, memory devices, I/O devices, interfacing, designing with microprocessors, debugging techniques.

Program design and analysis- models of program, assembly and linking, compilation techniques, analysis and optimization of execution time, energy, power and size.

Processes and operating systems- multiple tasks and multiple processes, context switching, scheduling policies, inter-process communication mechanisms.

Section 5: Analog &Digital CMOS ICs

Amplifiers: Common Source, Source follower, Common Gate and Cascode amplifiers, Biasing Techniques

Differential Amplifier: Basic differential Pair, common mode response, CMRR, Differential Pair with MOS load, Gilbert Cell.

Current Mirror: Basic Current Mirrors, Cascode Current mirror, Active Current mirror

CMOS Inverter:Timing, switching, and power analysis.

Combinational Circuits: Design of basic gates in NMOS technology; CMOS logic design styles: static CMOS logic (NAND, NOR gates), complex gates, Pass Transistor logic, Transmission gate, Dynamic MOS design: pseudo NMOS logic, clocked CMOS (C2 MOS) logic, domino logic, NORA, Half and Full adder), Multiplexer, XOR, XNOR.

Logical Effort: Logical Effort of Different Digital Circuit Design, Input capacitance, Logical and Electrical effort, parasitic delay.

Sequential MOS Logic and Memory Design: Static latches; Flip flops & Registers, Dynamic Latches & Register.

Model Questions:

1) A transistor is a …… operated device
   a) current
   b) voltage
   c) both voltage and current
   d) none of the above

2) Switching threshold voltage of an ideal CMOS inverter is defined as
   a) Vth = VDD/3
   b) Vth = VDD/2
   c) Vth = VDD
   d) Vth = VDD/4

3) Which design allows the reuse of the software and the hardware components?
   a) Memory Design
   b) Input design
   c) Platform-based design
   d) Peripheral design

4) Reverse recovery time affect the switching operation of
   (a) BJT (b) FET
   (b) MOSFET (d) All of the above