TEQIP –III, Sponsored 20 Hours Online Workshop
On

"Skill Development Workshop for Verilog/System Verilog"

15th to 23rd October, 2020 and
1st to 11th November, 2020

Organized by

Department of Electronics & Communication Engineering
MNIT Jaipur

Patron
Udaykumar R Yaragatti
Director, MNIT Jaipur

Convener
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Important Date
Last date of registration:
11th -October-2020, 5:00 PM
Link to the registration form:
https://forms.gle/3CvnNxFm3mBZSpDJ6

Registration Charges:

- No charges for MNIT Jaipur students
- Rs. 200/- for outside MNIT students
- Rs. 500/- for faculty

Online Payment Details:
A/c Name: The Registrar MNIT, Jaipur (TEQIP Phase-III)
Bank Name: State Bank of India (SBI)
Current A/c No.: 36875887782
IFSC Code: SBIN0015921
Branch Name: MNIT Campus, Jaipur
OR
PAYTM to +91-8426890515 (Rajinikanth R.)

Eligibility/Target Audience

- Faculty members/PhD Scholars/UG/PG Students of AICTE affiliated institutes.
- Applications will be accepted on **First cum first serve basis**.
- Certificates will be issued to the participants only after attending the complete course.

Twenty hours **skill development workshop for Verilog/System Verilog** in two phases from from 15th to 23rd October 2020 and 1st to 11th November 2020 is organised by **Department of Electronics and Communication engineering, Malaviya National Institute of Technology Jaipur**. MNIT Jaipur is ranked 35th in NIRF 2020 among Top Engineering Institutions in India. This workshop aims for Verilog/System Verilog for digital design and verification to make students much more employable in the field of Digital design and verification. The workshop will cover areas such as Digital design using Verilog and demonstration using opensource softwares, Verification methodologies OVM, UVM, System Verilog for design verification . The major goal is to offer all the essential theoretical as well as practical knowledge in the field of digital design and design verification. A comprehensive grading mechanism shall be devised based on the quizzes and mini project to make the participants understand concept in a better way.

Topics to be Covered: (approx. 4 hours per module)

Module 1: Verilog Modules [5 Hours] -VLSI Design flow, Concept of HDL, Features of HDL, Elements of HDL, Arrays in HDL, Basic Operators, Design styles of Verilog, Blocking and Non blocking assignments

Module 2: Testbench using Verilog [3 hours] -Basics of Test bench, Timing Semantics, Behavioral simulation, Non synthesizable code format

Module 3: FPGA architectures and Implementation (4 Hours) -PLD concepts, FPGA basic components, 7 series architecture, Synthesis & simulation, Implementation

Module 4: System Verilog [5 Hours] -Syntax in System Verilog, Basic concepts of System Verilog, Randomization, assertion, Coverage

Module 5: Verification Environment [3 hours] Components of Verification Environment (VE), Development of VE, Methodology of VE, Examples

** Industry experts will guide for job opportunities in VLSI domain

About the Department ECE

The department of Electronics and Communication Engineering started functioning in 1984. The department offers four-year courses leading to the Bachelor's Degree and also offer four Post Graduate Programs. It offers Ph.D. programs in various specializations like Artificial Intelligence, Device modelling, MEMS devices, optoelectronics, Antenna, RF-microwave, Wireless Networks, Image Processing, etc. The Department is equipped with state-of-the-art labs to support the UG, PG and Research Programs.

Venue/Mode:

The workshop will be organized using online **Platform**. The joining link and minute to minute time table will be shared one day before the workshop.

Speakers

Nidhi Agrawal
Staff Engineer at Qualcomm, M.Tech from IIT Kanpur

Dr. Amit Mahesh Joshi, Department of ECE, MNIT Jaipur

Dr. Menka Yadav Department of ECE, MNIT Jaipur

(Other reknowned speakers are contacted and will be added after confirmation at their end)

NOTE- Contact to coordinators for any query regarding the workshop.