Organized by
Electronics & ICT Academy

MNIT Jaipur
http://www.mnit.ac.in/eict

Methodologies and Challenges in Digital IC and Memory Design

Dec 11 - 15, 2019
Venue: Academy, Prabha Bhawan, MNIT Jaipur
http://www.mnit.ac.in/eict

Faculty Development Programme
Sponsored by

Department of Electronics & Information Technology
Ministry of Communications & Information Technology
Government of India

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Preamble (Electronics & ICT Academy)
Government of India had announced a National Policy on Skill Development, which has set a target of skilling 500 million people by 2022 in the domain of Electronics & IT. Under the plan scheme of "Digital India Manpower Development". MeitY has set up seven (07) Electronics and ICT Academies as a unit in 03 IITs, 03 NITs and 01 IIIT with an objective of faculty/mentor development/up gradation in the areas related to Electronics & ICT leading ultimately to improved employability of graduates/diploma holders. MNIT Jaipur has set up such an academy for providing specialized training to faculty and industry persons in the states/UTs of Rajasthan, Gujarat, Daman & Diu, Dadra Nagar Haveli.

(A) Issues-
1. IT Hardware and Electronics Manufacturing industry- availability of properly trained, skilled and qualified manpower
2. Number of quality PhDs generated in IT / Computer Science is very low
3. In E & ICT domain- there is a very high degree of obsolescence of existing technologies and faster emergence of newer technologies

(B) Approach-
1. A focused faculty training/updation programme for IT, Electronics and related sectors
2. Spreading up and continuous updation regarding Emerging Technology
3. Training and consultancy services for Industry
4. Design, Develop and Deliver specialized modules for specific research areas and Industry
5. Providing advice and support for technical incubation and entrepreneurial activities

An intensive one-week training programme is being organized for faculty of engineering and technological institutions. It is also open to faculties, persons from industry and doctoral students of Indian organizations. The objective is to provide an exposure to the participants to the state-of-the-art tools in Digital IC and Memory Design through interaction with experts from industries SCL, Chandigarh and academic CFTI institutions such as IITs/NITs/IIITs including host institution. The technical program will include mostly hands-on lab sessions, tool demonstrations, and discussion/presentation sessions with few lectures.

Programme Topics
A. MOSFET Overview, SPICE Model, DC & AC Characteristics.
B. VLSI fabrication Process, implementation strategies for Digital ICs.
C. Layout Design techniques, Synthesis, design of sense amplifier, Decoder.
D. Introduction to SRAM Architectures, SRAM memory controller and design Aspect.

Invited Experts –
Senior Scientists from SCL Chandigarh having more than 10 years of experience in Memory design and Chip fabrication would be the external resource persons for above FDP.

Programme Coordinators:

Prof. D. Boolchandani	dboolchandani.ece@mnit.ac.in	9549654229 (M)
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Registration:
Registration is open to faculty, industry persons, doctoral and postgraduate students of programmmes related to Electronics and Communication/ Electrical Eningeering. Participants will be admitted on a first-come first-served basis. Selected participants will be notified on or before 5 December 2019. Register on line at http://www.mnit.ac.in/eict

Fee:
(A) The one-time registration fee of Rs. 500/- would be applicable for each participant attending first time, irrespective of affiliation. This fee is not applicable for those participants, who have attended Academy training programme earlier.
(B). (i) The participants from academia and research scholars are required to pay a further fee of Rs. 2000/- (faculty/research-scholars). Rest expenditure is sponsored by DeitY through Electronics & ICT Academy at MNIT Jaipur.
(B). (ii) However, the participants from industries, UG/PG students would pay a further fee of Rs. 5000/-.
(C). The fee covers the participation in the programme, registration material including tutorial notes, boarding (breakfast/lunch) on all the days of the workshop. The travel and other expenses would have to be borne by the participants or their parent organizations.
(D). Lodging for very limited number of outside participants is available on first-come first-served and additional payment basis.
(E) The organizers should receive the registration amount through online payment/NEFT/IMPS/DD.

Account Name- 'Electronics and ICT Academy MNIT Jaipur'	Account Number- 676801700483
Bank address- ICICI Bank, MNIT Campus Branch, Jaipur	IFSC Code- ICIC0006768

(F) Please pre-intimate your desire to participate through e-mail, before registration form reaches us.
→For any other query else then this FDP, **email us at** academy@mnit.ac.in