Organized by
**Electronics & ICT Academy**

**MNIT Jaipur**
http://www.mnit.ac.in/eict

# Advances in

# VLSI Design Verification

**16th – 20th December 2017**
**Venue: Prabha Bhawan, MNIT Jaipur**
http://www.mnit.ac.in/eict

**Faculty Development Programme**
**Sponsored by**

Department of Electronics & Information Technology
Ministry of Communications & Information Technology
Government of India

Ministry of Electronics & Information Technology
Government of India
meity.gov.in/content/schemes-projects

**Chairman, Advisory Board,** EICT Academy & Director MNIT Jaipur
Prof. Udaykumar R. Yaragatti

**Academic Chair**, EICT Academy
Prof. V. Sinha

**Chief Investigator**, EICT Academy
Prof. Vineet Sahula, ECE

**Co- Chief Investigators**, EICT Academy
Dr. L. Bhargava, ECE
Dr. Pilli Emmanuel Shubhakar, CSE
Dr. C. Periasamy, ECE
Dr. S. J. Nanda, ECE
Head, ECE (Prof. K. K. Sharma)
Head, CSE (Dr. Girdhari Singh)

**Preamble (Electronics & ICT Academy)**
Government of India had announced a National Policy on Skill Development, which has set a target of skilling 500 million people by 2022 in the domain of Electronics & IT. Under the plan scheme of "Digital India Manpower Development". DeitY has set up seven (07) Electronics and ICT Academies as a unit in 03 IITs, 03 NITs and 01 IIIT with an objective of faculty/mentor development/up gradation in the areas related to Electronics & ICT leading ultimately to improved employability of graduates/diploma holders. MNIT Jaipur has set up such an academy for providing specialized training to faculty and industry persons in the states/UTs of Rajasthan, Gujarat, Daman & Diu, Dadra Nagar Haveli.

**(A) Issues-**
1. IT Hardware and Electronics Manufacturing industry- availability of properly trained, skilled and qualified manpower
2. Number of quality PhDs generated in IT / Computer Science is very low
3. In E & ICT domain- there is a very high degree of obsolescence of existing technologies and faster emergence of newer technologies

**(B) Approach-**
1. A focused faculty training/updation programme for IT, Electronics and related sectors
2. Spreading up and continuous updation regarding Emerging Technology
3. Training and consultancy services for Industry
4. Design, Develop and Deliver specialized modules for specific research areas and Industry
5. Providing advice and support for technical incubation and entrepreneurial activities

An intensive one-week training programme is being organized for faculty of engineering and technological institutions. It is also open to persons from industry and doctoral students of Indian organizations. The objective is to provide an exposure to the participants to the state-of-the-art in **Design Verification** of **Digital VLSI subsystems** through interaction with experts from **Texas Instruments, Bengaluru**. The technical program will include state-of-the-art lectures, hands-on lab sessions, tool demonstrations, and discussion/presentation sessions

| Topics | Modules (All engaged by Dr. C. P. Ravikumar) |
|---|---|
| Day-1: | Verification and its role in the VLSI design flow |
| Days 1 and 2: | Circuit-level verification |
| Days 3 and 4: | Gate-level and RTL verification (Verilog) |
| Day 5: | System-level verification (System Verilog,) |

**Invited Experts –**
**Dr. C. P. Ravikumar**, Director, Technical Talent Development, Texas Instruments, Bengaluru

**Programme coordinators**

| | | |
|---|---|---|
| Prof. Vineet Sahula | vsahula.ece@mnit.ac.in | 9549654 227 (M) |
| Dr. Amit M. Joshi | amjoshi.ece@mnit.ac.in | 9549654 239 (M) |

**Registration**
Registration is open to faculty, industry persons, doctoral and postgraduate students of programmmes related to **Electronics and Communication/ Computer Engineering**. Participants will be admitted on a *first-come first-served basis*. Selected participants will be notified on or before 05th December 2017.
Register on- line at http://www.mnit.ac.in/eict/apply_now.php

**Fee**
(A). The one-time registration fee of Rs. 500/- is to be paid by each participant attending first time, irrespective of affiliation. This fee is not applicable for those participants, who have attended any Academy training programme earlier.
(B). (i) The participants from academia and research scholars are required to pay a further fee of Rs. 2000/- (faculty/research-scholars). Rest expenditure is sponsored by DeitY through Electronics & ICT Academy at MNIT Jaipur.
(B). (ii) However, the participants from industries, UG/PG students would pay a further fee of Rs. 5000/-.
(C). The fee covers the participation in the programme, registration material including tutorial notes, boarding (breakfast/lunch) on all the days of the workshop. The travel and other expenses would have to be borne by the participants or their parent-organizations.
(D). Complimentary lodging for a very limited number of outside participants is available in Guest-rooms of Aurobindo-hostel. Also, accommodation in Guest-House-2 can be arranged, on *first-come first-served and additional payment basis.*
(E) The organizers should receive the registration amount through online payment/NEFT/IMPS/DD.

| | |
|---|---|
| Account Name-<br>'Electronics and ICT Academy MNIT Jaipur' | Account Number-<br>676801700483 |
| Bank address-<br>ICICI Bank, MNIT Campus Branch, Jaipur | IFSC Code-<br>ICIC0006768 |

(F). Please pre-intimate your desire to participate through e-mail, before registration form reaches us.

**Further query:**
(a) Please visit us at: http://www.mnit.ac.in/eict,
http://academymnit.wordpress.com
(b) Email us: academy[AT]mnit.ac.in